A 1.9GHz SINGLE-CHIP RF FRONT-END GaAs MMIC FOR PERSONAL COMMUNICATIONS

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ABSTRACT

A single-chip RF front-end GaAs MMIC for the 1.9GHz Japanese Personal Handy-phone System (PHS) is presented. RF circuits of a high power amplifier (HPA), a T/R switch (SW), two attenuators (ATTs), and a low-noise amplifier (LNA) are integrated ,with digital circuits of a negative voltage generator (NVG) for HPA and SW gate bias, and a logic circuit to control RF circuits.

The HPA has an output power of 21.5dBm and a high efficiency of 35% with sufficient linearity. The T/R SW combined with receive step-ATT (0/20dB) has loss of 1.2dB (include ATT 's loss) . The LNA has a gain of 11dB with noise figure of 1.7dB, which is self-biased to sleep negative voltage generator during receive mode. The IC needs only single voltage (+3V) DC power supply, and has logic interface to control each modes for TDMA/TDD scheme.

INTRODUCTION

With the recent worldwide progress in mobile personal communication system, the requirements for reducing size and manufacturing cost of RF circuits, has made the development of complete T/R subsystems integrated in a single-chip. This paper describes a single-chip RF front-end GaAs MMIC for the 1.9GHz Japanese Personal Handy-phone System (PHS). Fig. 1 shows a photograph of the MMIC.

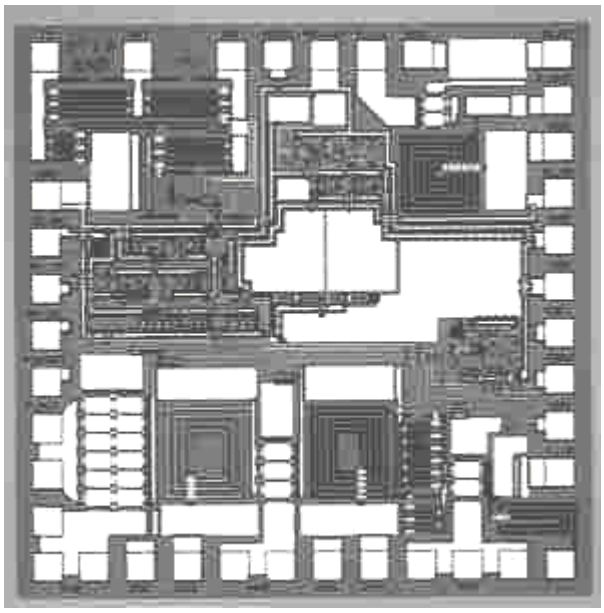

Fig. 1 Photograph of the MMIC

MMIC ARCHITECTURE

The 1.9GHz Japanese PHS employs $\pi/4$ shift QPSK modulation, the Time Division Multiple Access(TDMA) and the Time Division Duplex(TDD) scheme. The bit rate and channel spacing are set at 384kbps and 300kHz. The required output power of handheld is 19dBm at antenna port. The architecture of the RF front-end MMIC for

PHS is shown in Fig.2. The IC consists of a high power amplifier (HPA), a SPDT switch for TDD operation, a low noise amplifier (LNA), a RX attenuator to prevent LNA from saturation caused by excessive input signal, a TX attenuator for HPA power control, a negative voltage generator (NVG) for HPA and SW gate bias, and logic circuits which controls above components. The IC needs single DC power supply of +3V, and has logic interface to control each modes for TDMA/TDD system.

The E- and D-mode FETs are implemented as active device using a state of the art SAGFET process technique [1] .

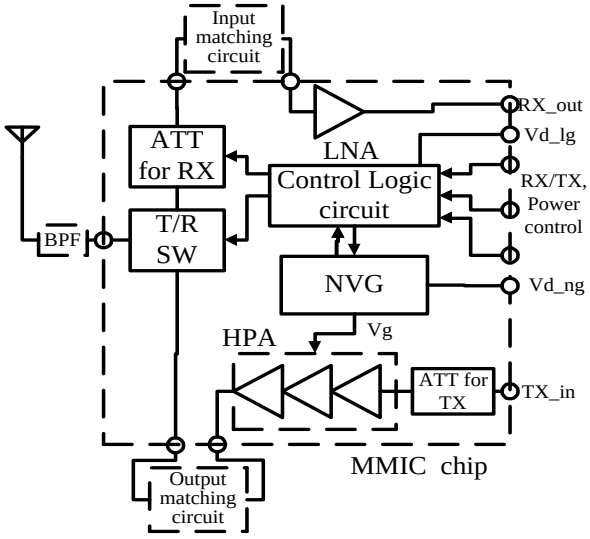

Fig.2 RF front-end MMIC for PHS

HIGH POWER AMPLIFIER

The high power amplifier has three-stages. The gate peripheries of the 1st, 2nd stages are 0.4 and 0.6mm respectively. The gate periphery of final stage FET is 2.4mm to obtain an output power of 21dBm with low-distortion (less than -55dBc of adjacent channel leakage power with π/4 shift QPSK). The load impedance and source impedance for the final stage FET is determined for high efficiency with low distortion[2]. The interstage matching circuits are included in the MMIC chip, the output matching circuit is assembled outside of the MMIC chip in order to reduce GaAs chip size and matching loss. The FET used in HPA and SW has high pinch-off voltage and break down voltage to achieve high efficiency and high handling power.

Fig. 3 shows input-output power, ACP (Adjacent Channel leakage Power) and power added efficiency for π/4 shift QPSK modulated signal. An HPA has an output power of 21.5dBm with ACP of -55dBc and associate gain of 35dB. A Power added efficiency of 35% have been obtained. The HPA output spurious caused by the negative voltage generator (NVG) is as low as -70dBc [2].

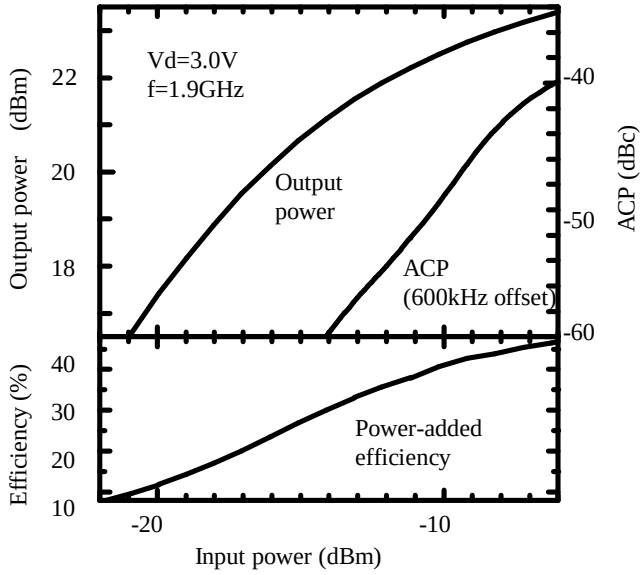

Fig.3 Output power, ACP and efficiency for π/4 shift QPSK modulated signal

T/R SWITCH AND ATTENUATOR

Fig. 4 shows a schematic diagram of T/R switch(SW) and RX attenuator (RX-ATT) portion. At TX port, the SW consists of conventional series and parallel FETs, at RX port SW and RX attenuator are combined to reduce chip size and RF loss. The RX attenuator prevent LNA from distorting with

excessive input signal. The RX-ATT is composed SW-FET and resistances (R1, R2, R3). The gate periphery of series FET is determined to obtain insertion loss of ATT less than 0.6dB. R1 and R3 are determined considering on resistance of the ON-state FET. Drain and source of FETs are pulled up to 3V. At transmitting mode, negative voltage for gates of off-state FETs are biased to have handling power of more than 22dBm. At receiving mode, the gate bias is 0V to sleep the NVG , thus the DC power consumption is significantly reduced. At transmitting mode, the RX-ATT is in the attenuation state. To realize high attenuation at attenuation mode, the capacitor at ground port are optimized so as to cancel the inductance of ground wire at 1.9GHz. The IC has also a TX-attenuator for power control. It is π-type step attenuator of 0/20dB.

Fig. 5 shows measured insertion loss of the SW/RX-ATT at transmitting, receiving, and attenuation modes. At attenuation mode, 17dB of insertion loss has been obtained. The isolations are more than 20dB at all states. Fig. 6 shows input power versus loss of SW/RX-ATT. With NVG (Vg=-1.6V), the SW has handling power of more than 22dBm .

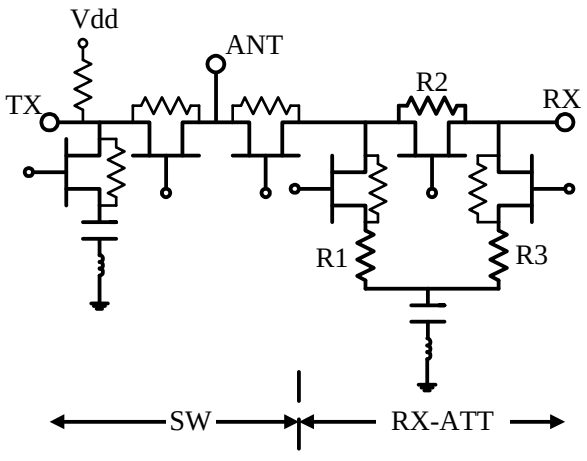

Fig. 4 Schematic diagram of SW/RX-ATT

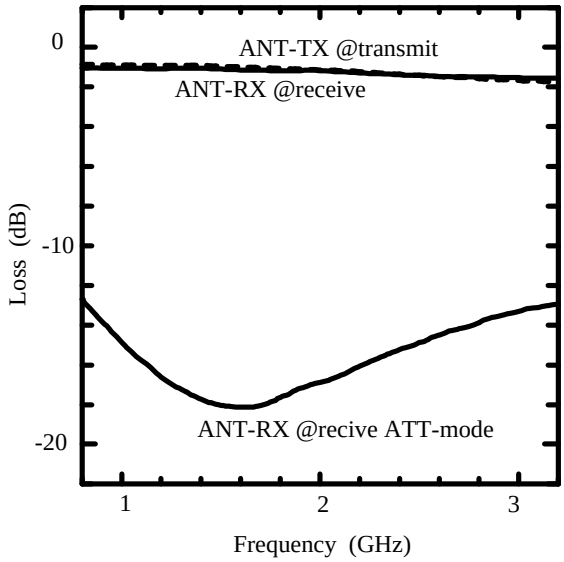

Fig. 5 Insertion loss of SW/ATT

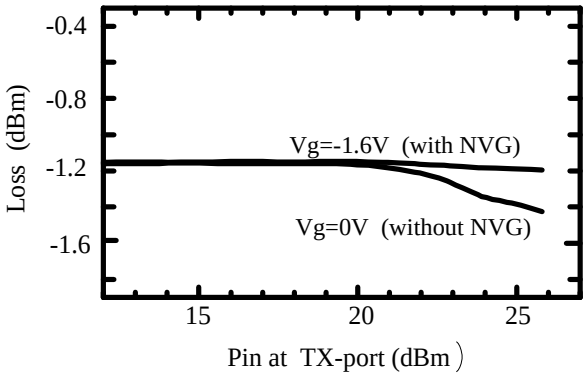

Fig. 6 Input power versus loss of SW/ATT

LOW NOISE AMPLIFIER

To low power consumption and high gain, the FET for the LNA has low pinch-off which is used as D-FET in NVG and logic circuits. A conventional self-bias circuit is employed for single voltage operation, because NVG dose not work during receiving mode for low power consumption. Output matching circuit consists in the chip, on the other hand, input matching circuit may be formed out of MMIC chip to save chip size and matching loss.

The LNA has noise figure of 1.7dB, gain of 11dB and a input S11 of -13dB. Fig. 7

shows S-parameter of the LNA. The consumption current is 5mA with 3V.

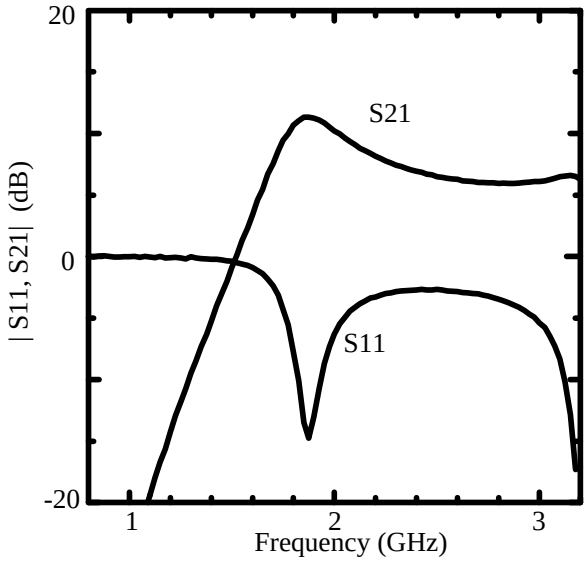

Fig. 7 S-parameters of LNA

NEGATIVE GENERATOR

The Negative Voltage Generator (NVG) is comprised of a multivibrator, two drivers, two charge pump circuits, and a level control circuit [3]. It has very low ripple negative voltage output, which is suitable for biasing the HPA.

The circuit generates negative voltage of -1.6V for SW, -1.2V for HPA gate bias. The deviation of the gate bias is suppressed within 0.1V for FET gate current of 120μA or less. The current consumption of NVG is as low as 2.3mA

CONTROL LOGIC CIRCUIT

The control logic has three modes for the Time Division Multiple Access (TDMA), the Time Division Duplex (TDD) scheme, that is transmitting, receiving, and stand-by modes. Each mode has attenuation states which depend on radio signal level. The logic circuit controls NVG , SW bias and ATT bias. The consumption current of the circuit is less than 0.8mA at all modes

CONCLUSION

We have demonstrated the single chip RF front-end GaAs MMIC for digital mobile communication system, such as Japanese Personal Handy-phone System. It has an HPA optimized for high efficiency with sufficient linearity, and a T/R switch combined with receive step attenuator, a low noise amplifier, and a negative voltage generator, and logic circuits for control above circuits. The IC needs single voltage DC power supply, and logic interface. The consumption current with 3V DC supply is totally 140mA, 6mA, 1mA for transmit, receive, sleep modes, respectively. The HPA has a output power of 21.5dBm, associate gain of 35dB and efficiency of 35%. The T/R SW has high handling power of more than 22dBm with assistance of negative voltage generator. The self-biased LNA has noise figure of 1.7dB and gain of 11dB. These features are suited to Japanese PHS application.

REFERENCES

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